

# Electrostatic discharge of charged electronic modules

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## Abstract

Electrostatic discharges (ESD) of charged electronic printed wiring board assemblies and encapsulated electronic modules are of growing importance due to many industrial cases where such discharges have resulted in numerous device failures of electrostatic origin for the assemblies/modules. In this paper, basics of such discharges, commonly called Charged Board Model (CBM) electrostatic discharges, are reviewed and methods for the ESD control of CBM type of discharges are presented.

**Keywords:** electrostatic discharge, ESD, Charged Board Model, CBM, electronic assemblies, electronic modules

## 1. Introduction

The evolution of semiconductor technology and electronics has led to devices where semiconductor element dimensions are smaller than ever before, in minimum only a few atomic layers. Unfortunately, this evolution has made many devices extremely vulnerable to disturbances of electrostatic origin. Thanks to effective protection circuits, however, most semiconductor devices can withstand electrostatic discharges from a human being charged to 2 kV without any failure. Nevertheless, there are many devices with Human Body Model (HBM) withstand voltage of only a few hundreds of volts [1-3], or even less than 100 V, and a safe handling of such devices is not possible without an effective ESD control program.

While the attention of ESD protection has been focused on HBM type of ESD with successful results, another important type of electrostatic discharge, namely the discharge of charged device (Charged Device Model ESD, CDM) or charged printed wiring board assembly (Charged Board Model ESD, CBM), has often been left aside the interest. Recent failure reports from electronics manufacturing as well as from repair show rapid increase of device or equipment failures of electrostatic origin for assemblies and modules which have high ESD robustness against HBM ESD. Further analyses of the failures often reveal that the reason for a failure has been a rapid discharge of charged board assembly or encapsulated module directly to ground or to another high capacitive conductive structure. Such ESD failure reports are usually

confidential, but Olney et al. at Analog Devices published in 2003 an important study on that [4]. They concluded that a device, when assembled on a board, can be much more susceptible to CDM/CBM type of ESD failure than as a stand-alone device. After that, similar board level failures at unexpected low charging voltages have been semi-confidentially reported by many companies handling ESD sensitive electronics during manufacturing, assembly or repair.

In this paper I will focus on the electrostatic discharges of charged electronic modules at large. The results are applicable for electronics as well as automotive industry where open board assemblies or encapsulated electronic modules are handled. At first, the Charged Board Model ESD is described and defined in more detail and, then, some example cases of CBM ESD are shown. Methods for the evaluation of ESD susceptibility of electronic assemblies/modules are discussed and, finally, basic ESD protective actions to minimise ESD failures of CBM type are given.

## **2. Charged Device Model and Charged Board Model ESD**

Charged Device Model (CDM) is a standard expression for an ESD event that occurs when a charged component abruptly touches another metallic object or surface at a different electric potential [5,6], see Fig. 1(a). The component is charged either by induction due to electrostatic field from nearby charged insulators or by triboelectrification due to rubbing (contact) with another material. In a CDM discharge the direction of ESD current is from the device to lower potential (ground), which is opposite to Human Body Model (HBM) and Machine Model (MM) ESD. Furthermore, the duration of a CDM ESD is typically 1-2 orders of magnitude shorter than that of a HBM ESD, so that CDM is a nanosecond event. These result in that the ESD protection circuits designed to protect the device from the HBM type of ESD may not be fully effective in a CDM discharge.

An electrostatic discharge of an entire charged board assembly or electronic module is different to that of a single device in so many aspects that experts have started to use a different expression for that, namely Charged Board Model (CBM) ESD. Commonly used, but not standardised, definition for CBM is that Charged Board Model is an ESD event that occurs when a populated charged printed wiring board abruptly touches another metallic object or surface at a different electric potential, Fig. 1 (b). The board is charged by induction or triboelectrification similarly to the CDM case. The speed of a CBM ESD is similar to the CDM case (that is in the nanosecond range), but in a CBM ESD a major part of ESD current flows through the ‘victim’ device like in a HBM ESD.

A typical CBM case is that semiconductor devices of the electronic module (board assembly) become, at first, charged by induction due to the vicinity of highly charged plastic material, which could even be the plastic cover of the module. The discharge of the charged devices (as well as charged board conductors) happens when the module is assembled on its place and connected to the conductors of equipment. The peak discharge current in a Charged Board Model (CBM) ESD can easily be several Amps due to the large capacitance of the board assembly with large amount of charge stored in the conductors of the board.

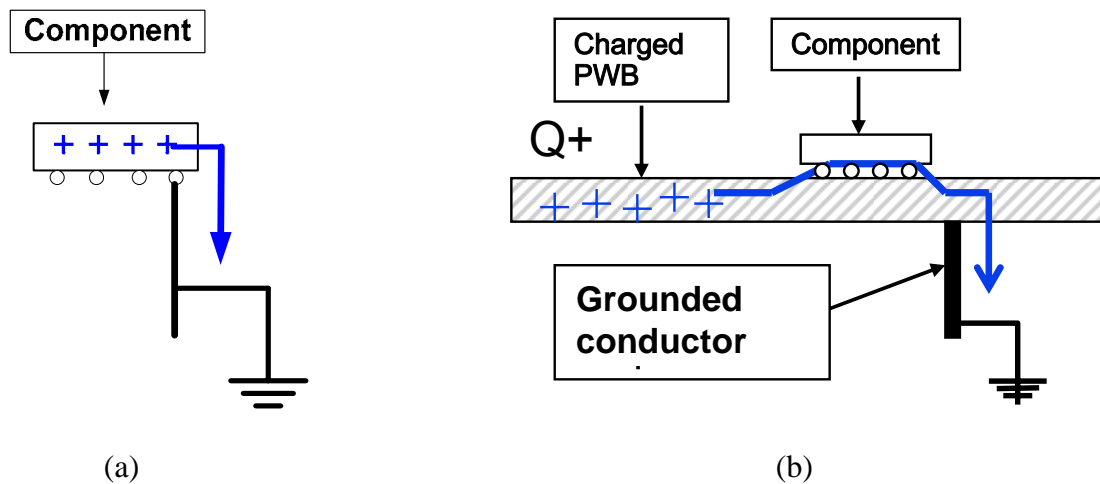


Figure 1 Principles of (a) Charged Device Model (CDM) ESD and (b) Charged Board Model (CBM) ESD.

### 3. Example cases of CBM ESD

In this chapter two example cases of CBM ESD are presented. They both represent published studies done at laboratories. Both studies, however, were initiated by real industrial problem cases where ICs that are robust to ESD at the component-level were damaged by ESD at the board-level at board/module voltages well below to their reported standard ESD withstand voltages.

The first study was carried out at Analog Devices, Inc. [4]. A customer of Analog Devices experienced a very high failure rate (6.7%) on a CMOS Dual Op Amp IC, in a board assembly, at charging levels (board charging) well below the HBM and CDM withstand voltages of the device, which were  $V_{\text{HBM}} = 3000 \text{ V}$  and  $V_{\text{CDM}} = 1500 \text{ V}$ , respectively. At board-level testing reproducible device failures happened already at  $-500 \text{ V}$  (charging level of the board assembly/module). CBM stressing of fresh samples at higher voltages resulted in severe damage that could easily be mistaken for EOS (electrical overstress) damage. The duration of the CBM ESD was less than  $1 \text{ ns}$  and the CBM ESD peak current was about 3x CDM peak current: at  $375 \text{ V}$  the CBM peak current was  $6 \text{ A}$ . At the lower ESD levels, CBM ESD led to a partial device failure giving rise to malfunctions which may or may not be seen during final equipment testing. At the higher ESD levels, CBM ESD led to a catastrophic device failure noticed in equipment testing. For more details of the example case, see ref. [4].

The second study was carried out at VTT (and published in part in ref. [7]) in order to understand the ESD problem of a customer of VTT during the assembly stage of electronic module and in order to solve the problem. The experiments included 3 different kinds of modules with both unpopulated versions (prints) and populated versions (full modules). ESD currents were measured at different charging voltages and at different distances from a ground plane for constant charge.

Basic equations which link the voltage,  $V$ , the charge,  $Q$ , and the energy,  $E$ , of the module together are

$$V = \frac{Q}{C}, \quad (1)$$

$$E = \frac{1}{2} CV^2 = \frac{1}{2} \frac{Q^2}{C}, \quad (2)$$

where  $C$  is the capacitance of the module conductor. The equations demonstrate the importance of (varying) capacitance in determining the risk of ESD damage to sensitive devices in charged board type of ESD. Measurements may show, for example, low voltage due to suppression by nearby machine parts or a grounded mechanic (high  $C$  case). In another part of the manufacturing line the same electronic module carrying the same charge may indicate much higher voltage because of changed board capacitance (low  $C$  case). The difference between low and high voltage level of a module in a line may easily be tenfold for a constant charge. It has been shown [8,9] that in CBM ESD failure voltages of devices reduced with increasing board capacitance, and that ESD energy would be a proper threshold for damage instead of voltage. In the VTT studies below, either  $C$  or  $Q$  was in turn kept constant and the other parameter was varied in order to understand the dependencies between the major parameters  $V$ ,  $Q$ ,  $C$ , and  $E$  in real CBM discharges.

Example CBM discharge current waveforms are given in Fig. 2 at different charging voltages of the module while  $C$  was kept constant. From the figure we can see that CBM peak currents depend linearly on the charging voltage. All discharges in Fig. 2 were taken at the same test point of the module. A CBM discharge taken at another test point of the module could be somewhat different but typically still within the same range. Differences between module types, however, were significant, underlining the important influence of the board capacitance (i.e. the capacitance of board conductor) on the ESD waveform. Differences between unpopulated (prints) and populated modules were also significant. For unpopulated boards (prints) the peak ESD current in a CBM discharge was typically about 50% smaller than for the corresponding populated module at the same charging voltage (applies in the cases of the study). The duration of the discharge was always small, a few ns.

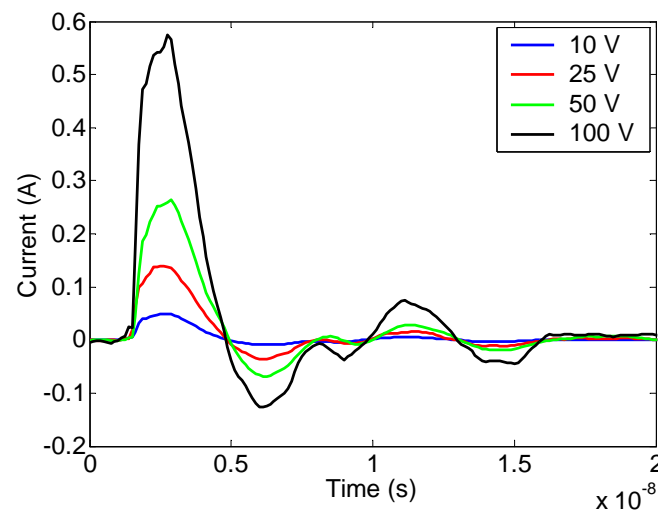


Figure 2 ESD current waveforms of a charged electronic module discharged to short at different initial charging levels: (from the bottom to the top) 10 V, 25 V, 50 V and 100 V.

In a manufacturing (and repair) environment the board/module capacitance and voltage are seldom constant. Typically a charge may arise on a module that may be considered nearly constant over certain transport stages, and the voltage and capacitance of the module change along with the movement of the module and proximity to grounded machine parts or mechanics. The case of varying board to ground plane distance for a constant charge is presented in Fig. 3. The (floating) board was charged to 100 V (~1 nC) at a 80 mm distance between the board and ground plane. The distance between the board and ground was then decreased and discharge was initiated and measured. In Fig. 3, ESD current waveforms are shown for distances of 80 mm, 70 mm, 50 mm, 35 mm, 20 mm, 12 mm and 8 mm. From the discharge current waveforms we can see that the peak current decreases along with decreasing distance (and increasing capacitance); At the same time, according to Eqs. (1) and (2), when the capacitance increases, ESD voltage (i.e. module potential) and ESD energy decreases. The behaviour is vice versa at increasing module-to-ground distance for a constant charge (not shown here).

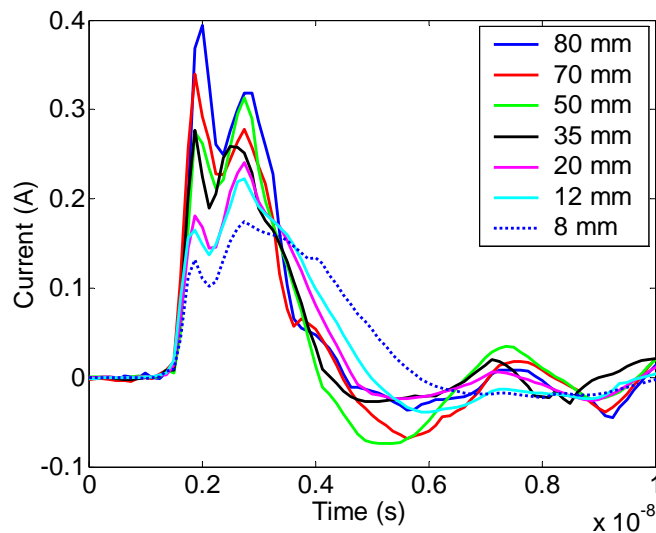


Figure 3 CBM discharge currents for an electronic module, charged to 100 V (1 nC) at 80 mm, at various distances between the board and ground plane (from 80 mm on the top to 8 mm on the bottom).

#### 4. Assessment of risks of device damage

In the case of Charged Device Model (CDM) ESD, the standard CDM withstand test data gives a good estimate for ESD safe handling of the device (stand-alone devices – not assembled on a board). The standard CDM test does not give accurate information because the test is not sufficiently well specified and there can be differences between testers from different manufacturers leading to differences in test results. Nevertheless, the CDM test gives a good and often worst case estimate of the device CDM withstand. It is important to mention here that the CDM discharge is fundamentally very different to the HBM discharge and, therefore, there is no general correlation between HBM and CDM withstand levels of devices. Accordingly, HBM test data gives little support for the assessment of risks of device damage due to CDM ESD.

The CBM ESD case is again very different to the CDM case and there is no general correlation between CDM and CBM withstand levels of devices. Because an ESD from a populated board assembly depends strongly on the product, no standard test data or test procedure is defined. It is possible to do CBM withstand tests for a product (and we have at VTT done such studies), but estimates of board or module level ESD withstand are typically based on the HBM, MM, or CDM test data of devices on the board.

A common myth is that the ESD damage threshold of a populated board/module is equal to that of the most sensitive device on the board. While this may be true for a HBM type of ESD, it is not true for CBM type of ESD. There are several reasons for that. At first, if we compare CDM and CBM, the large capacitors and multilayer board structures of board assemblies (or electronic modules) can store much more charge than a single device can. More charge may mean a stronger ESD. On the other hand, while the direction of discharge current in a CDM is outwards from the device, in a CBM the discharge current flows largely through the device and, therefore, on-chip ESD protection operates differently in the CDM and CBM cases. If compared to HBM, the direction of discharge current is largely similar in the HBM and CBM cases, but the duration of CBM discharge is 1-2 orders of magnitude shorter than that of HBM discharge. That means thermodynamically very different kind of situation in the failure region (see ref. [10] for a more detailed discussion on the subject). One can conclude that it is difficult to ‘precisely’ estimate the ESD withstand of a populated board assembly against CBM discharge, but an experience has shown that the CBM withstand of the board is usually much less than the CDM withstand of the most sensitive device on the board.

There have been published some methods to estimate the ESD withstand of a populated board assembly against CBM discharge using standard device test parameters [7,10,11]. The most commonly used approach for a rough worst case estimate is based on the use of standard Machine Model (MM) test data of the devices on the board [11]. CBM discharges are like MM ESD external to the device that is threaten because the charge is mainly stored on the capacitance of the board conductors. Supposing that all the energy stored in the board, Eq. (2), is deposited directly in the victim device, the worst case CBM threshold voltage,  $V_{CBM}$ , would be given by [11].

$$V_{CBM} = V_{MM} \sqrt{\frac{C_{MM}}{C_{CBM}}}, \quad (3)$$

where  $V_{MM}$  is the MM withstand voltage of the most sensitive device on the board (from device test data),  $C_{MM}$  is the MM capacitance (200 pF), and  $C_{CBM}$  is the capacitance of the board assembly. The practical problem is that  $C_{CBM}$  is not constant but depends on the position of the board with respect to its environment (ground). Even if the  $C_{CBM}$  is not fixed or known, it is almost always less than  $C_{MM} = 200$  pF, which means that  $V_{CBM} > V_{MM}$ .

Experience has shown that, even when the  $C_{CBM}$  is known, true  $V_{CBM}$  is higher than that given by Eq. (3). In Eq. (3) it is assumed that all the ESD energy is dissipated solely in the failure region, but in practice the discharge energy is distributed over the

resistive structures of the discharge path, the failure region often still being the location of major energy dissipation.

## **5. Minimisation of ESD failures due to CBM ESD**

The major international standards for the protection of electronic devices from electrostatics phenomena – IEC 61340-5-1 [5] and ANSI/ESD S20.20 [6] – are intended to cater for electronic components, assemblies and subassemblies with a Human Body Model sensitivity of 100 V or greater. Accordingly, they give necessary guidance to protect ESD sensitive devices from dangerous ESD from human beings. They may not directly give necessary guidance for the ESD control in the case where the risks of ESD failures are due to the discharge of charged electronic modules. However, the general principles of ESD prevention with an EPA (ESD Protected Area) of the standards are equally important in the prevention ESD failures due to CBM discharges. The general principles of ESD prevention are:

- All conductors are equipotential bonded (and preferably grounded)
- All non-essential insulating materials are excluded
- Materials and equipment designed for use have carefully controlled charge generation and dissipation properties
- Where insulating materials are necessarily present, the charge on these is minimised by measures such as ion neutralisation.

In the minimisation of device failures due to CBM discharges of electronic modules, there are two complementary strategies (after the basic ESD protective actions of the standard ESD control programs [5,6] have been implemented): at first, the charging of modules should be minimised and, secondly, any low-ohmic contact from the module conductor to ground should be avoided. The charging of modules by induction can be avoided by excluding all non-essential insulating materials and high voltages near (less than 30-50 cm) from the module, and if process essential insulating materials are present, the charge on these is minimised by ionisation or the charging effect is minimised by electrostatic shielding. Charging by triboelectrification (rubbing) can be minimised, in the case of encapsulated modules, by using electrostatic dissipative or conductive surface cover in the encapsulation, whenever functionally possible.

In practice, the charging of modules cannot be completely avoided in a typical manufacturing environment. Therefore, a special attention should be paid to the handling of electronic modules. When handling charged modules, one should avoid direct low-ohmic contacting to the conductors of the module (I/O pins, power leads, ground, board wiring, etc.). The contact should be done, whenever possible, by electrostatic dissipative material. The ideal surface resistance range of materials contacting the module conductor is from  $1 \times 10^6 \Omega$  to  $1 \times 10^9 \Omega$ . The lower resistance limit comes from the requirement to offer sufficient damping for the peak discharge current in order not to cause any failure for extremely ESD sensitive devices. For more ESD robust devices, a lower limit of  $1 \times 10^5 \Omega$  is sufficient (in some cases even  $1 \times 10^4 \Omega$  is sufficient to damp the current to a safe level). The upper resistance limit comes from the requirement that the charge generated on/in the module could be safely dissipated during the time in contact. The  $1 \times 10^9 \Omega$  is a safe limit for automatic handling. For manual operations the upper limit can be higher,  $1 \times 10^{11} \Omega$  (or in some

cases even  $1 \times 10^{12} \Omega$ ). In assembly and testing stages, the process often requires low-ohmic electrical contact to the module. In such cases, the charge stored on/in the module should be safely discharged by contacting the module conductor with a grounded electrostatic dissipative material prior to module assembly or testing. In these stages, one should always handle modules like they were charged and do the safe module discharging prior to the low-ohmic contacting.

## 6. Conclusions

Charging of electronic modules (printed wiring board assemblies) is of great concern during manufacturing, assembly and repair stages of electronics. Due to the higher capacitance of an electronic module, if compared to a typical stand-alone device, more charge can be stored in the module. That results in a risk for strong and destructive ESD if the charge stored in/or the module is rapidly discharged. While the standard ESD protective actions recommended in the ESD control standards are effective for preventing ESD failures due to charged operators and machines, they may be insufficient to prevent ESD failures due to CBM discharges. Therefore, some additional elements must be added to the ESD control program of a company for an ESD safe handling of electronic modules.

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