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Assessment of ESD threats to electronic components and ESD control requirements

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Abstract. We propose new methods for the assessment of real electrostatic discharge (ESD) threats to electronic components in modern electronics manufacturing environment, where the devices are more sensitive to ESD than ever. The work was based on two fundamental questions: what are the key parameters of ESD that must be controlled in order to minimise risk of damage, and what are the threshold levels of these parameters, below which ESD risk is low? As a result of the study, proposals are given for two new ways of assessing risk: by measurement of peak ESD current, and charge induced on test objects. We suggest how guideline limits for ESD damage thresholds based on these tests may be derived.

1. Introduction

In modern electronics manufacture ESD (electrostatic discharge) sensitive electronic devices, such as discrete transistors and integrated circuits, may be at risk from damage from ESD from objects and materials in their environment. Typical ESD sources include operators, charged insulators and isolated metal parts in automated handling equipment and manual assembly, including clothing of operators. Effective ESD control to minimise device failures due to ESD in modern electronics manufacturing environment requires that real ESD threats to electronic components are well assessed.

ESD waveforms are highly variable, and ESD sensitivity in components must be assessed using an ESD model that appropriately simulates the real world ESD waveform. Historically, this has led to the development of three main component ESD withstand test models: Human Body Model (HBM), Machine Model (MM) and Charged Device Model (CDM) [1,2,3]. Standard tests are now listed by bodies such as the ESD Association, JEDEC and the IEC and are regularly used in qualification of production electronic device designs.

Device ruggedness specified as HBM, MM and CDM withstand voltage may be found on some modern device data sheets. Device manufacturers commonly include protection networks in IC designs, targeted at achieving 2kV HBM, 200V MM, and 1kV CDM ESD withstand voltage thresholds. However there are many devices that are unprotected and have ESD withstand voltages less than 1kV. RF technologies commonly have HBM and MM withstand in the 30 - 200 V range. Giant MagnetoResistive (GMR)

heads are probably the most sensitive devices currently available, with ESD withstand voltages in the Volt region.

In practice, these ESD withstand voltages are a poor guide to ESD risk in the manufacturing environment. Voltage is a consequence of the charge and its environment, rather than being a fundamental contributor to ESD risk. When a charged printed wiring board is transported along a conveyor, measurements may show low voltage due to nearby metallic machine parts. In another part of the machine the same board carrying the same charge may indicate a much higher voltage [4]. A device ESD withstand voltage indicates the risk of damage only under a particular set of circumstances with a particular model ESD source. The risk of ESD damage of devices due to charged insulators near or in contact with a device cannot be assessed well by using any voltage criterion.

There is a need to identify more realistic and quantifiable parameters than voltage for assessing ESD risk. The objective of this paper is to propose ESD risk thresholds that are related to the real device damage mechanisms, in terms of practical measurable parameters such as peak ESD current and charge storage on ESD sensitive devices.

2. Human Body Model, Machine Model and Charged Device Model ESD withstand

The Human Body Model (HBM) simulates the situation where a charged person touches a device, with another pin of the device typically grounded. Machine Model (MM) emulates the situation where a charged metallic object (such as a trolley or charged machine part) is the ESD source. Both types of event are "2-pin" events where a discharge current enters one pin and leaves another, passing through device internal circuitry.

The situation is simulated using a simple electronic circuit (Figure 1). Additional components may need to be added to tailor the waveform to better represent real world waveforms [2]. A capacitor C is charged to an ESD voltage V_{esd}. On initiating the ESD event, the ESD current flows through a circuit resistance R, inductance L and the load device (and possible spark gap). Typical component values are shown in Table 1. The largest voltage V_{esd} that the device can stand without damage is the device ESD withstand voltage.

HBM and MM ESD typically create the same types of damage signatures in the component, even though the ESD waveforms are very different [2,3]. The peak current achieved by HBM is achieved at much lower ESD voltage in MM due to the lower circuit impedance, which consists primarily of stray L and R, and the impedance of the victim device. For the same ESD voltage, MM ESD currents are about 10-20 times the HBM value. Perhaps not surprisingly, the ESD withstand voltage for MM is found to be 10-20 times less than HBM. The duration of HBM and MM ESD is typically 100-150 ns.

In the Charged Device Model (CDM) the victim device itself acts as the circuit capacitor. C is now the device effective capacitance (a variable), and the L and R are stray components within the discharge path.

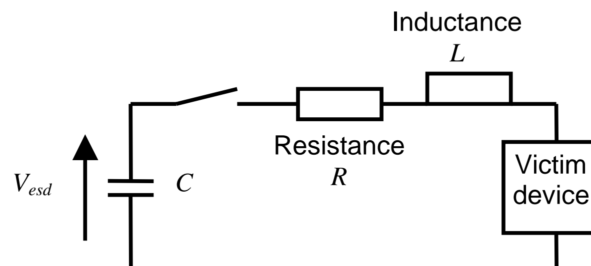

Figure 1. A general ESD model.

Table 1. Typical ESD model simulation component values

Model	R (Ω)	C (pF)	L (nH)
Human body model HBM	1500	100	stray
Machine model MM	stray	200	stray
Charged device model CDM	< 10	Capacitance of device under test (1-30pF)	< 10

CDM ESD damage typically has different failure signatures than HBM and MM. CDM ESD occurs when a device becomes charged, and then is brought into contact with a low impedance ground. The discharge is a "1-pin" event with the discharge current originating in the device, and limited by the ground path and device internal impedances. A short duration (a few ns), high current (higher than in MM) waveform results.

Charged device model is of growing importance, especially in automated handling and assembly systems where a device may become charged by triboelectrification or induction from nearby fields, and subsequently contact metal machine parts.

3. Component damage due to energy dissipation in internal weak components

In HBM and MM, damage of ESD sensitive devices often occurs because a small internal region is intensely heated by the passage of the ESD current. The damage region may be a metallization track, or a transistor junction.

The power dissipation in the damage region is given by

$$P(t) = I(t)^2 R(t)$$

where *P(t)*, *I(t)* and *R(t)* are the instantaneous power dissipation, discharge current and effective device resistance. The power dissipation causes a temperature rise in the region – damage is caused if the temperature exceeds a certain threshold (e.g. the material melting point). Modern devices have extremely small (sub micron) internal feature dimensions, and so only a small energy is required to raise the hot spot to the damage temperature.

Models of this failure mode have been based on the general heat flow equation

$$\rho C_p \frac{dT}{dt} - K\nabla^2(T) = q(t)$$

where ρ is the density, C_p is the specific heat, T the temperature of the material, K is the thermal conductivity, and $q(t)$ is the rate of heating per unit volume of the heat source. Smith has argued that a general heat equation of this type applies for all ESD failures including metal, semiconductors and insulating materials [5].

Wunsch & Bell [6] developed the first junction burnout model based on the solution of the heat flow equation for a planar heat sorce, considering the temperature rise ΔT of the junction to the fail temperature. Tasca [7] extended the Wunsch-Bell model to wider time regimes and solved the heat flow equation for a spherical source in an infinite medium. The reader is referred to Tasca's original work for details. In Tasca's solution power P_f required to raise the spherical region to fail temperature is a function of the pulse duration

$$P_f = \left(\frac{AV}{t} + \frac{BS}{\sqrt{t}} + C \right)(T - T_0)$$

where $A = \rho C_p$ and V is the volume of of the heat source, $B = (K\rho C_p)^{1/2}$ and S the surface area of the heated region, C is a constant describing the steady state condition, T is the temperature of the device and T_0 is the initial temperature. The equation above shows that the power required to failure for a given failure temperature is determined by the duration of

the discharge pulse. For short pulses ($t < 0.1$ µs) the situation is adiabatic (i.e. there is no or very little heat flow out of the heated region) and the time dependence follows an $1/t$ dependence. In this regime, a constant amount of energy $AV(T-T_0)$ is required to raise the spherical region to failure temperature, dependent only on the size of the heated region, properties of the materials, and the temperature rise to failure. In the regime of intermediate pulse lengths (0.1µs to 100 µs) some heat diffuses away from the defect region and the failure power $BS(T-T_0)$ follows a $t^{-1/2}$ dependence. For long pulse ($t > 100$ µs) energy is lost to the surrounding material at a constant rate (dependent on device heat sinking) and, thus, the failure power is constant. In summary, the power required to reach the failure temperature decreases as t is increased until a steady state is achieved.

4. Proposal of a discharge current threshold for ESD damage

For ESD damage to occur, the internal power dissipation in the weak region must exceed a threshold value to overcome heat losses from the region. This power dissipation must occur at some discharge current level, and a current threshold for ESD damage therefore is proposed.

If this current level is exceeded the power dissipation will rapidly exceed the power required to heat the damage site to the damage temperature ($P=f(I)$) and providing the discharge is of sufficient duration, damage will occur. An ESD event having a lower peak current can be expected to not exceed the power threshold, and therefore not cause damage. A threshold obtained for a longer duration discharge, where power loss from the heated region is significant, can be expected to give a safe value for shorter ESD durations.

One question is, how can the threshold be measured? We do not know where the weakest region in the device may be, or what is its size or effective resistance.

In the HBM ESD withstand test the discharge current is primarily governed in many, if not most, cases by the series 1500 Ω resistance. The duration of the discharge is about 100 ns, which is likely to be on the threshold of the adiabatic heating regime. We can propose that the peak current in the HBM ESD event may directly give a reasonable measure of the ESD current threshold for damage of the device in HBM & MM-like situations. Perhaps most usefully, the test is already performed on the majority of devices. If the device HBM withstand voltage V_{HBM} is known, then an appropriate peak ESD current threshold I_{ESDmax} can be calculated from

$$I_{ESD\max} = \frac{V_{HBM}}{1500}$$

Thus a threshold of 100 V HBM gives a peak current threshold of 66.7 mA. Protection of 10 V HBM devices requires a reduction in peak current threshold to 6.7 mA. In general, the allowable current is 0.67 mA per Volt HBM withstand.

One complication is that a real HBM waveform includes an initial transient due to the discharge of stray circuit components. This transient will tend to make the device fail at a lower HBM ESD threshold voltage. This, however, would lead to underestimation of the ESD current withstand threshold, which increases the margin of safety for ESD risk assessment when using the calculated peak current as a damage threshold.

In assessing an ESD garment material, or and automated handling line, for ESD risk, the HBM ESD withstand peak current is therefore a primary specification. The material or equipment should not be able to source an ESD peak discharge current exceeding this threshold. A survey of such discharges may be made part of the material or equipment laboratory qualification procedure.

5. Proposal of a charge threshold for ESD damage

Some authors have also found evidence that CDM withstand voltage is related to peak ESD current [8, 9]. However, the peak current is a result of device and discharge circuit impedance as well as the ESD voltage. So, it is very much a device package, situation and environment dependent parameter. It is not easy to see how peak discharge current can realistically be used as a failure threshold in this case. The HBM values do not apply, as the failure modes are typically different, for example due to internal oxide layer breakdown.

5.1. Proposal of a charge limit from the CDM test parameters

The CDM peak current is likely to be a function of CDM voltage arising on the device capacitance. So, it is reasonable to propose a charge threshold could be defined, with ESD damage risk occurring when charge induced on, or accumulated by the device reaches and exceeds this value. Charge measurement is relatively easy and a device independent test can be envisaged. The device CDM voltage withstand V_{CDM} is a standard test result, and coupled with a device capacitance value C_d could yield a charge threshold value Q_{th}

$$C_d V_{CDM} = Q_{th}$$

One problem is, what value of C_d should be used? Device capacitance is seldom measured, and in practice varies with the device position and surrounding materials and objects. If the capacitance in the CDM test configuration is known, this would be an appropriate value. More often, the capacitance is not known. The obvious approach is to choose a value at an extreme of the range, although it is not initially clear whether a high or low value presents the safest choice. Device capacitance is often in the range 1 – 30 pF for integrated circuits.

5.2. Specification of a charge threshold

The CDM peak current is determined by the series resistance and inductance of the circuit. These are stray components of indeterminate value, inherent in the device structure. Two key questions are, can we justify linking peak current and device charge level, and if so, what combination of V_{CDM} and C_d could give the highest peak current? We can simplify the argument by considering each series component in turn. If the series resistance R is sufficiently large that the effect of the inductance is negligible, the peak current I_p is given by

$$I_p = \frac{V_{CDM}}{R}$$

Clearly this is greatest when V_{CDM} is maximum. Substituting for charge

$$I_p = \frac{Q_{th}}{C_d R}$$

Thus the peak current is proportional to the device charge level, and for a given device charge level, the highest value of I_p is found at minimum device capacitance. Similar result can be obtained for the case where the resistance is negligible compared with the inductance.

From this analysis, choosing a low value for C_d would give a safe estimate for use in charge threshold calculation. A value of 1 pF would represent a small device at the lower end of the possible range. Most devices sensitive to CDM ESD would be expected to have higher capacitance than this. While a small device in free space could have a lower capacitance, ESD risk is only present when a device approaches an object and the capacitance is greater than the free space value.

If the CDM withstand voltage V_{CDM} of the most sensitive device expected handled is known we can use this value, otherwise we might choose a low value of, say, 100 V. The calculated charge threshold for these estimated values is then 0.1 nC. Induced charge or triboelectrically generated charge less than this value would not be expected to cause CDM damage to most devices. In practice a variety of factors in any case reduce the ESD risk. If a greater margin of safety is required, then the charge threshold may be reduced accordingly.

The analysis is supported by the results of Brodbeck and Kagerer [8] who have shown that device charge levels at the damage threshold reduced with reducing device capacitance, although the peak current at the threshold level remained the same.

6. Conclusions

Two new methods of assessment of ESD risk to sensitive electronic devices have been proposed here, with proposals of how appropriate limits may be derived from standard ESD test results. In summary the proposals are that

- Discharge current, power and energy related damage thresholds can be simplified to be represented by an ESD peak current threshold for damage which covers a wide range of situations with a margin of safety. The peak discharge current threshold is derived from component HBM ESD sensitivity data
- A charge threshold can be derived that corresponds to ESD risk to a charged device. The threshold may be derived from standard CDM ESD sensitivity data.

Further work is in progress to evaluate the usefulness of the approach in practice, applied to assessment of ESD garments and automated manufacturing facilities. We anticipate that the proposals may find more general application in many different situations in electronics manufacture.

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